In the Specification

Amend the following numbered paragraphs of the specification:

[0019] Fig. 2 is a schematic block diagram representation according to a first embodiment of the invention showing a portion of a memory array, wherein an existing external signal "read cycle n+1" is combined with a "conventional precharge signal" in an AND-gate thereby generating a new precharge signal for a respective array segment; and

[0023] Referring again to Fig. 1, the broken lines in the bitline true (BLT) and bitline complement (BLC) timing signatures show the benefit achieved by the present invention. Namely, that the bitlines are not precharged when a write access follows a read or write access. For example, broken lines A and B in the BLT and BLC signals indicate that the bitlines are not precharged when a write access follows after a read access as further indicated by broken line C. However, benefits can only be achieved when the data, associated with that specific ~~bitlines~~ bitline does not change its value from cycle n to cycle n+1. Thus, no power savings between t4 and t5 are achievable.

[0031] While the invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is understood that ~~numerour~~ numerous other modifications and variations can be ~~dfevised~~ devised without departing from the scope of the invention.